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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/487,969	01/18/2000	Maria Clemens Y. Quinones	18865-35US	3787

20350 7590 12/31/2002

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EXAMINER
CHAMBLISS, ALONZO

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/487,969	QUINONES ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Amendment A filed on 10/4/02 has been fully considered and made of record in Paper No. 7. Therefore, claims 1-6 have been canceled.

Response to Arguments

2. Applicant's arguments filed on 10/4/02 in Paper No. 7 have been fully considered but they are not persuasive.

Applicant alleges Williams et al. does not disclose all of the features recited in the claims such attaching a bumped die that includes a source and gate solder bump array. This argument is respectfully deemed to be unpersuasive because Williams discloses a bumped die 358 (i.e. MOSFET) includes a source and gate solder bump array that is attached the bottom lead frames 304, 344, since these bumps are attached to a gate lead 408 and source metal 410 (see col. 17 lines 31-53). A MOSFET includes a source and gate region as described in Figs. 7A and 7B).

Applicant alleges Williams et al. and Ishibashi do not disclose reflowing the solder as recited in claim 10, 20, 26, and 28. This argument is respectfully deemed to be unpersuasive because Williams discloses solder bumps 342 attached to the top lead frame 344 (see Fig. 16C). One skilled in the art would readily recognize using a reflow process on solder bumps, since a reflow process enables the solder material to melt and form a good electrical connection between lead frames and printed circuit boards. Therefore, one skilled in the art would readily recognize using a reflow process of the solder bumps with the process of Williams, since the reflow process enables the solder

material to melt and form a good electrical connection between lead frames and printed circuit boards.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 7, 8, 13-16, 21-24, 29, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (U.S. 6,307,755) in view of Watanabe (U.S. 5,365,106).

With respect to Claims 7, 15, and 23, Williams discloses a plurality of bottom lead frames 304, 344 coupled to one another with a pair of rails 304C and a plurality of top lead frames 3)02, 348 coupled to one another with a pair of rails 302C (see Figs. 14D

and 16C). Fig. 14D shows a portion of a plurality of lead frames which can be seen by section 11 in Fig. 3E. A bumped die 358 (i.e. MOSFET) includes a source and gate solder bump array that is attached the bottom lead frames 304, 344, since these bumps are attached to a gate lead 408 and source metal 410 (see col. 17 lines 31-53). A MOSFET includes a source and gate region as described in Figs. 7A and 7B). The top lead frames 344 are flipped such that each top lead frame contacts the solder bumps 342 on a corresponding bumped die 358. The bumped die 358 is between each the top lead frames 348 and corresponding bottom lead frames 344 (see Fig. 16C).

With respect to Claims 8, 16, and 24, Williams discloses a molded body 350 is placed around each top and bottom lead frame 344, 348 with a corresponding bumped die 3 58 between them (see Fig. 16C).

With respect to Claims 13, 14, 21, 22, 29, and 30, Williams discloses the bumped die 358 is attached to the bottom lead frame 348 with an adhesive (i.e. soft solder or conductive epoxy), wherein the adhesive is cured sometime during the method after the die 358 is attached to the lead frame 348 (see col. 17 lines 25-29).

With respect to Claims 31-33, it is well known when having a pair of rails coupling the bottom lead frames include aligners (i.e. positioning holes) and the pair of rails coupling the tope lead frames include corresponding holes, and wherein when the top lead frames are flipped onto the bottom lead frames, the aligners and holes are used to ensure proper alignment as evident by Watanabe col. 2 lines 65-68 and col. 3 lines 1-4; Fig. 3).

Claims 9-12, 17-20, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (U.S. 6,307,755) as applied to claims 7, 15, and 23 above, and further in view of Ishibashi (U.S. 5,394,751).

With respect to Claims 9, 11, 17, 19, 25, and 27, Williams fails to disclose spot welding to create a press-fit between the rail of the bottom lead frame and a rail of the top lead frame together. However, Ishibashi discloses spot welding to create a press-fit between the rail of the bottom lead frame and a rail of the top lead frame together (see col. 4 lines 10- 15). Therefore, it would have been obvious to use the spot welding technique with Williams, since the spot welding technique would increase the rigidity of the die pad portion of the lead frame as taught by Ishibashi.

With respect to Claims 10, 12, 18, 20, 26, and 28, Williams discloses solder bumps 342 attached to the top lead frame 344 (see Fig. 16C). One skilled in the art would readily recognize using a reflow process on solder bumps, since a reflow process enables the solder material to melt and form a good electrical connection between lead frames and printed circuit boards. Therefore, one skilled in the art would readily recognize using a reflow process of the solder bumps with the process of Williams, since the reflow process enables the solder material to melt and form a good electrical connection between lead frames and printed circuit boards.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

AC

AC/December 28, 2002